**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Previously Presented) A programmable logic device (PLD) including:

at least first and second logic array blocks (LABs);

a plurality of first signal lines capable of driving the second LAB;

a plurality of output lines driven by the first LAB; and

a first swap multiplexer (MUX) having a first selectable input capable of being driven directly by at least one of the plurality of output lines and a second selectable input capable of being directly driven at least one of the plurality of the first signal lines, and an output capable of driving the at least first LAB.

2. (Previously Presented) The PLD of claim 1 wherein:

the first LAB includes a first plurality of logic elements (LEs) and the second LAB includes a second plurality of LEs;

at least one of the plurality of output lines is driven by at least one of the first plurality of LEs;

at least one of the plurality of the first signal lines is capable of driving at least one of the second plurality of LEs; and

the output of the first swap MUX is capable of driving at least one of the first plurality of LEs.

3. (Original) The PLD of claim 2 wherein:

the first LAB includes a plurality of local lines at least one of which drives at least one of the first plurality of LEs; and

the output of the first swap MUX drives at least one of the plurality of local lines.

4. (Original) The PLD of claim 3 further including at least one additional signal line for exclusively driving the second LAB.

5. (Previously Presented) The PLD of claim 4 wherein the plurality of first signal lines include a plurality of LAB lines which drive the second LAB and a plurality of tap lines at least one of which is interconnected with at least one of the plurality of LAB lines, at least one of the plurality of tap lines driving the first selectable input of first swap MUX.

6. (Original) The PLD of claim 5 wherein the interconnection between the at least one LAB line and at least one tap line is fixed.

7. (Original) The PLD of claim 6 further including at least a third LAB and a plurality of second signal lines capable of driving the third LAB wherein the first swap MUX includes a third selectable input and at least one of the second signal lines drives the third selectable input.

8. (Original) The PLD of claim 6 further including:

at least a third LAB and a plurality of second signal lines capable of driving the third LAB;

a second swap MUX having a first selectable input and second selectable input the first selectable input capable of being driven by at least one of the second signal lines; and

wherein the plurality of tap lines include a first set of tap lines and a second set of tap lines, at least one of the first set of tap lines capable of driving the first selectable input of the first swap MUX and at least one of the second set of tap lines capable of driving the second selectable input of the second swap MUX.

9. (Currently Amended) A programmable logic device (PLD) including:

at least first and second logic array blocks (LABs), the first LAB including a first plurality of logic elements (LEs) and the second LAB including a second plurality of LEs;

a plurality of first signal lines capable of driving at least one of the second plurality of LEs;

a plurality of output lines driven by at least one of the first plurality of LEs; and

a first swap multiplexer (MUX) having a first selectable input capable of being driven **directly** by at least one of the plurality of output lines and a second selectable input capable of being **directly** driven by at least one of the plurality of first signal lines, and an output capable of driving at least one of the first plurality of LEs.

10. (Original) The PLD of claim 9 wherein:

the first LAB includes a plurality of local lines which drive the first plurality of LEs; and

the output of the first swap MUX drives at least one of the plurality of local lines.

11. (Previously Presented) The PLD of claim 10 wherein the plurality of first signal lines include a plurality of LAB lines at least one of which drives the second LAB and a plurality of tap lines at least one of which is interconnected with at least one of the LAB lines, at least one of the tap lines driving the first selectable input of the first swap MUX.

12. (Original) The PLD of claim 11 further including at least a third LAB and a plurality of second signal lines capable of driving the third LAB wherein the first swap MUX includes a third selectable input and at least one of the second signal lines drives the third selectable input.

13. (Original) The PLD of claim 11 further including:

at least a third LAB and a plurality of second signal lines capable of driving the third LAB;

a second swap MUX having a first selectable input and a second selectable input the first selectable input capable of being driven by at least one of the second signal lines; and

wherein the plurality of tap lines include a first set of tap lines and a second set of tap lines, at least one of the first set of tap lines capable of driving the first selectable input of the first swap MUX and at least one of the second set of tap lines capable of driving the second selectable input of the second swap MUX.

14. (Previously Presented) A method of driving logic array blocks (LABs) in a programmable logic device (PLD) including:

providing at least first and second LABs in the PLD;

driving the second LAB with at least one of a first plurality of signal lines;

driving at least one of a plurality of output lines with the first LAB;

directly driving a first selectable input of a first swap multiplexer (MUX) with at least one of the plurality of output lines;

directly driving a second selectable input of the first swap MUX with at least one of the plurality of first signal lines; and

driving at least the first LAB with an output of the first swap MUX.

15. (Original) The method of claim 14 further including:

providing a first plurality of logic elements (LEs) in the first LAB;

providing a second plurality of LEs in the second LAB;

driving at least one of the plurality of output lines with at least one of the first plurality of LEs; and

driving at least one of the second plurality of LEs with at least one of the plurality of first signal lines.

16. (Original) The method of claim 15 including:

providing a plurality of local lines in the first LAB;

driving at least one of the first plurality of LEs with at least one of the plurality of local lines; and

driving at least one of the plurality of local lines with the output of the first swap MUX.

17. (Original) The method of claim 16 further including providing at least one additional signal line for exclusively driving the second LAB.

18. (Previously Presented) The method of claim 17 further including;

providing a plurality of LAB lines and a plurality of tap lines in the plurality of first signal lines;

driving the second LAB with at least one of the plurality of LAB lines; and

interconnecting at least one of the plurality of tap lines with at least one of the plurality of LAB lines;

driving the first selectable input of the first swap MUX with at least one of the plurality of tap lines.

19. (Original) The method of claim 18 further including fixing the interconnection between the at least one of the plurality of LAB lines and the at least one of the plurality of tap lines.

20. (Original) The method of claim 19 further including

providing at least a third LAB and a plurality of second signal lines;

driving the at least third LAB with at least one of the plurality of second signal lines

providing a third selectable input in the first swap MUX; and

driving the third selectable input with at least one of the plurality of second signal lines.

21. (Original) The method of claim 19 further including:

providing at least a third LAB and a plurality of second signal lines;

driving the third lab with at least one of the plurality of second signal lines;

providing a second swap MUX having a first selectable input and a second selectable input;

driving the first selectable input with at least one of the plurality of second signal lines;

including in the plurality of tap lines a first set of tap lines and a second set of tap lines;

driving the first selectable input of the first swap MUX with at least one of the first set of tap lines; and

driving the second selectable input of the second swap MUX with at least one of the second set of tap lines.